| Notice of Allowability | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/749,607 | ROESNER ET AL. | |
| | Examiner | Art Unit | |
| | Kandasamy Thangavelu | 2123 | |

***-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--***

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *December 15, 2006*.

2. ☒ The allowed claim(s) is/are *1-18*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

**Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 12/15/06
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

## DETAILED ACTION

### *Introduction*

1. This communication is in response to the Applicants' communication dated December 15, 2006. Claims 1, 7 and 13 were amended. Claims 1-18 of the application are pending.

### *Examiner's Amendment*

2. Authorization for this examiner's amendment was given in a telephone conversation by Mr. Brian Russell on February 12, 2007.

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to the applicants, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

3. In the claims:

In amended Claim 1, Line 21, "in accordance with the indication"

has been changed to

-- in accordance with the constraint information --.

In amended Claim 7, Line 1, "A data processing system"

has been changed to

-- A data processing system for compiling a simulation model of a digital design --.

In amended Claim 7, Line 2, "a processing resources"

has been changed to

-- processing resources --.

In amended Claim 7, Line 23, "in accordance with the indication"

has been changed to

-- in accordance with the constraint information --.

In amended Claim 13, Line 1, "A program product"

has been changed to

-- A program product for compiling a simulation model of a digital design --.

In amended Claim 13, Lines 2 and 3, "computer usable medium"

has been changed to

-- computer readable storage medium --.

In amended Claim 13, Line 23, "in accordance with the indication"

has been changed to

-- in accordance with the constraint information --.

## *Reasons for Allowance*

4. Claims 1-18 of the application are allowed over prior art of record.

5. The following is an Examiner's statement of reasons for the indication of allowable subject matter:

The closest prior art of record shows:

(1) a method, system and data structure for incorporating random instrumentation logic within a hardware description language simulation model; the circuit design is divided into smaller parts called design entities that are individually designed; the design entities are combined in a hierarchical manner to create an overall model; a reference model is written to process test vectors and produce expected results; the test vector is run on the simulation model by the simulator; verification programs are used at the simulation phase to monitor correctness and intermediate results; the method of instrumentation uses the hierarchical nature of the design to monitor performance characteristics of specific modules to efficiently identify failures and assess logical correctness of the models; instrumentation modules written in HDL are used to monitor specific design parameters; for each design entity a bill-of-materials lists the entity's descendants and the date and time of their creation; the bill-of-materials file is used by the compiler to determine which files should be updated during compilation; the compiler does incremental compiling using a recursive method; instrumentation modules provide for monitoring failure events, count events and harvest events indicating occurrence of specific circumstances (**Roesner et al.,** U.S. Patent Application 2002/0128809);

(2) a method and program product for instrumenting a hardware description language design entity; the circuit design is divided into smaller parts called design entities that are individually designed; the design entities are combined in a hierarchical manner to create overall model; the method of instrumentation uses the hierarchical nature of the design to monitor performance characteristics of specific modules to efficiently identify failures and assess logical correctness of the models; instrumentation models called the instrumentation entities are embedded within the design entities; instrumentation modules written in HDL are used to monitor specific design parameters; the compiler does incremental compiling using a recursive method; instrumentation modules provide for monitoring failure events, count events and harvest events indicating occurrence of specific circumstances (**Williams et al.,** U.S. Patent Application 2002/0120922); and

(3) method of instrumenting synthesizable source code to provide debugging support for gate level simulation; the method generates instrumentation data and instrumentation logic indicative of execution status of RTL source code statements; a modified gate level netlist is used to generate instrumentation signals corresponding to synthesizable statements within the source code; an execution count of cross referenced synthesizable statement can be incremented when the corresponding instrumentation signal indicates the statement is active to determine the source code coverage; source code statements can be highlighted when active for visually tracing execution paths (**Raynaud et al.,** U.S. Patent Application 2001/0011212).

None of these references taken either alone or in combination with the prior art of record discloses a method of compiling a simulation model of a digital design, specifically including:

(Claim 1) "receiving as an input into a model build process, constraint information indicating a desired set of instrumentation entities to be included within a simulation model of a digital design described by a plurality of hierarchically arranged design entities, wherein said instrumentation entities monitor logical operation of one or more of said plurality of design entities during simulation for occurrence of events of interest, wherein the desired set of instrumentation entities includes fewer than all instrumentation entities defined for the simulation model, and wherein said constraint information is distinct from source code files describing said plurality of design entities and said instrumentation entities defined for the simulation model".

None of these references taken either alone or in combination with the prior art of record discloses a data processing system for compiling a simulation model of a digital design, specifically including:

(Claim 7) "means for receiving as an input into a model build process constraint information indicating a desired set of instrumentation entities to be included within a simulation model of a digital design described by a plurality of hierarchically arranged design entities, wherein said instrumentation entities monitor logical operation of one or more of said plurality of design entities during simulation for occurrence of events of interest, wherein the desired set of instrumentation entities includes fewer than all instrumentation entities defined for the simulation model, and wherein said constraint information is distinct from source code files

describing said plurality of design entities and said instrumentation entities defined for the simulation model".

None of these references taken either alone or in combination with the prior art of record discloses a data program product for compiling a simulation model of a digital design, specifically including:

(Claim 13) "means for receiving as an input into a model build process constraint information indicating a desired set of instrumentation entities to be included within a simulation model of a digital design described by a plurality of hierarchically arranged design entities, wherein said instrumentation entities monitor logical operation of one or more of said plurality of design entities during simulation for occurrence of events of interest, wherein the desired set of instrumentation entities includes fewer than all instrumentation entities defined for the simulation model, and wherein said constraint information is distinct from source code files describing said plurality of design entities and said instrumentation entities defined for the simulation model".

6. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 571-272-3717. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez, can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to TC 2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PAUL RODRIGUEZ
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

2/14/07

K. Thangavelu
Art Unit 2123
February 12, 2007